## 32.9 A 16-to-18GHz 0.18μm Epi-CMOS Divide-by-3 Injection-Locked Frequency Divider

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Frequency dividers are essential building blocks in wireless and wireline communications as well as radar systems for functions such as frequency synthesis, quadrature signal generation, MUX/DEMUX, and bandwidth compression. An injection-locked frequency divider (ILFD) enjoys lower power dissipation and better noise performance than common digital dividers. However, their application is hindered by the limited locking range and division ratios. This paper addresses the latter problem.

A differential-*LC* oscillator has become a popular choice for ILFDs [1]. Such a differential-*LC* ILFD can be viewed as a special type of regenerative divider with a single-balanced mixer [2, 3]. Frequency division happens when the second-harmonic current is injected into the tail node and switched by the nonlinear differential pair to generate the mixing products. Then all harmonics except the fundamental frequency component are filtered out by the *LC* tank. Because the mixing function of the cross-coupled differential pair has odd symmetry, it only generates odd-order mixing products, which correspond to even frequency-division ratios (2, 4, 6 ...). In order to support divide-by-$(2n + 1)$ operation, it is necessary to change the topology of the built-in mixer. A straight-forward way is to use a single transistor, e.g., injection locking a Colpitts oscillator [1]. Due to the current-switching nature of MOSFET transistors, however, doing so results in small lock range. Using a single transistor also loses all the benefits of differential circuits. Injection-locked ring oscillators can also be used for divide-by-3 operation [4]. However, they do not provide filtering like a resonant oscillator, and hence tend to have large unwanted harmonic components, particularly at the injected signal frequency. They are also prone to lock at the wrong harmonics and their phase-noise performance is inferior to resonant ILFDs.

To address these problems and preferably maintain the differential *LC* oscillator topology, we construct a *cascode differential LC ILFD* by adding another differential pair: $M_3$ and $M_4$ (Fig. 32.9.1). $M_3$ and $M_4$ convert the differential injection signal into a differential current, which mixes with the differential output voltage signal by $M_1$ and $M_2$. Since $M_1$ and $M_2$ are no longer a differential pair, their even-order nonlinearity can generate the desired mixing product, which corresponds to an odd division ratio. A shunt-peaking inductor $L_0$ is also introduced to resonate with the parasitic capacitances at the 3rd harmonic [2]. It also provides a short-circuit current path for the fundamental component. Therefore, the upper half of the circuit ($M_1$, $M_2$, $L_0$ and the *LC* tank) works as a differential *LC* oscillator at the fundamental frequency, and the lower half ($M_3$, $M_4$, and $L_0$) as a tuned differential amplifier. So the differential topology is preserved, although mixing is accomplished in a single-ended fashion. Overall, we confine signals at different harmonics locally by circuit topology and filtering. A balun $T_1$ is used to convert a single-ended input from a signal source to a differential signal. It also helps to match the input impedance of $M_3$ and $M_4$ to 50Ω. The input can be directly connected when the ILFD is integrated with an on-chip differential source like a differential VCO.

A prototype ILFD with input frequency of 18GHz using the new topology has been designed and fabricated using a 0.18μm standard digital CMOS technology with low-resistivity epi substrate. Spiral inductors are constructed using the 0.9μm-thick top metal layer. Due to the thin metal layer and lossy substrate, the $Q$ of the inductors is 4 at 5GHz. Varactors $C_{t1}$ and $C_{t2}$ are built with NMOSFETs in inversion mode. An open-drain differential buffer is used at the output port. The ILFD core and output buffer consume 2.55mA and 22.6mA from a 1.8V power supply, respectively.

The prototype ILFD chip is measured by on-wafer probing. The loss from the cables, adaptors and probes between the signal source and the input port is characterized to calibrate the injected signal power. $S_{11}$ at the input port is measured and used to calculate the gate voltage on $M_3$ and $M_4$. $S_{11}$ is less than -8dB across the frequency tuning and locking range and the injected power is adjusted from the incident power accordingly. The output signal spectrum in the locked condition is shown in Fig. 32.9.2. The 2nd and 3rd harmonics are -23dB and -21dB below the fundamental frequency, and a large part of them is contributed by the open-drain buffer at the output (single-ended measurement). The locking range increases from 0.3GHz at an injected power of -14dBm, to 1GHz at 4dBm with little change in the center frequency (Fig. 32.9.3). The corresponding input port voltage is calculated using $S_{11}$ and is shown in Fig. 32.9.4. Note that this is the single-ended voltage (amplitude) at the primary of the balun with a 1:1 transformation ratio. The ILFD can also be tuned by the varactors $C_{t1}$ and $C_{t2}$ with the free-running frequency from 5.37 to 6.1GHz. The locking range shifts nicely with the free-running frequency and remains almost constant across the tuning range (Fig. 32.9.5). Hence the ILFD covers a 3.2GHz input frequency range, which can be further expanded by adding a switched capacitor bank.

Figure 32.9.6 shows the phase noise performance of the ILFD at different injected power levels. The phase noise of the free-running ILFD and the signal source are also shown for comparison. Due to the low $Q$ inductors, the free-running phase noise is not good at all. When the ILFD is in the locked condition, the phase noise follows that of the signal source with a 9 to 10dB reduction with large injected power (-3dBm and 3.7dBm), which matches well with the theoretical value 9.5dB. For small injected power (-8dBm), the phase noise degrades only at large offset frequency. At the edges of the locking range, it is found that the phase noise degradation is negligible at small offset frequency (<200KHz), while becomes noticeable at larger offset.

The die micrograph is shown in Fig. 32.9.7. The chip size is 0.9mm×0.9mm.

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*References:*
[1] H. Rategh and T. H. Lee, "Superharmonic Injection-Locked Frequency Dividers," *IEEE J. Solid-State Circuits*, vol. 34, pp 813-821, June, 1999.
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[3] S. Verma, H. R. Rategh and T. H. Lee, "A Unified Model for Injection-Locked Frequency Dividers," *IEEE J. Solid-State Circuits*, vol. 38, pp 1015-1027, June, 2003.
[4] W.-Z. Chen and C.-L. Kuo, "18GHz and 7GHz Superharmonic Injection-Locked Dividers in 0.25μm CMOS Technology," *Proc. ESSCIRC*, pp 89-92, 2002.

 

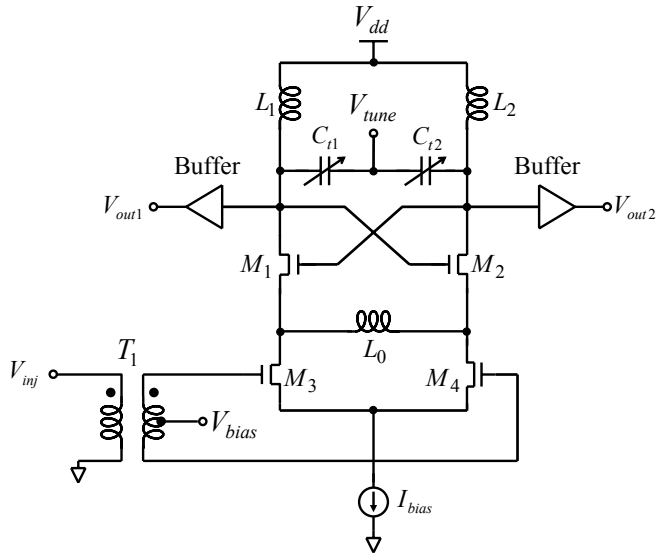


Figure 32.9.1: New divide-by-3 ILFD.

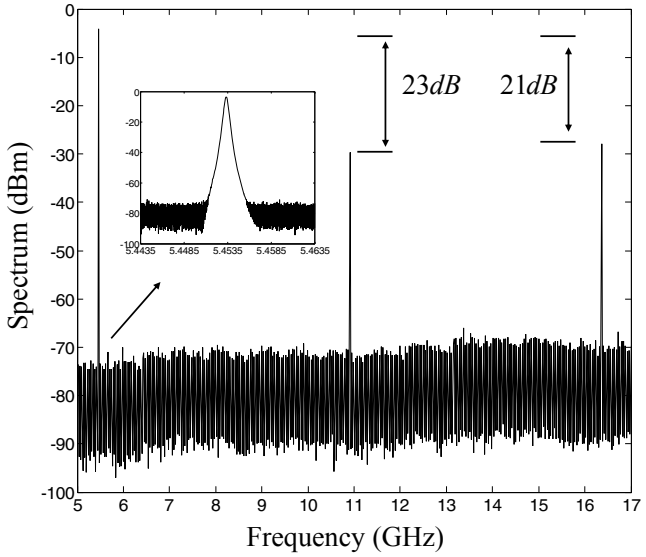


Figure 32.9.2: Measured output spectrum.

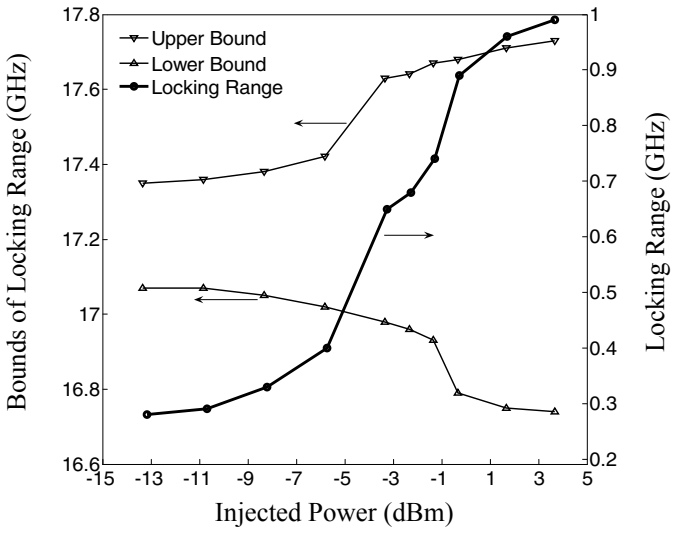


Figure 32.9.3: Measured locking range versus injected power.

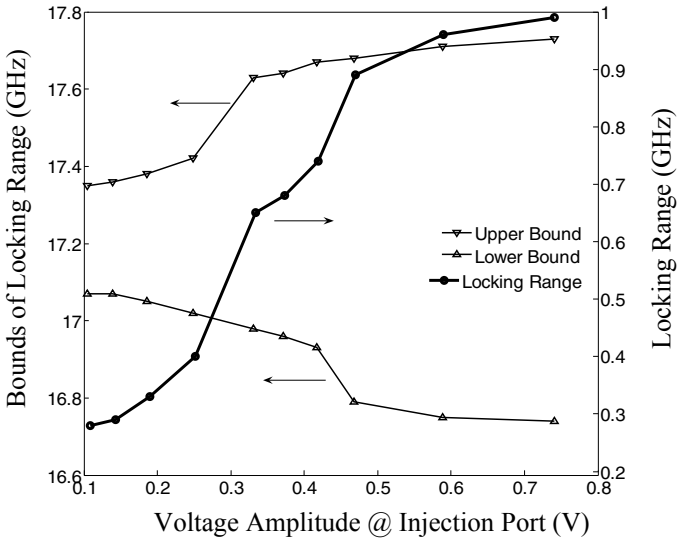


Figure 32.9.4: Measured locking range versus injection voltage amplitude.

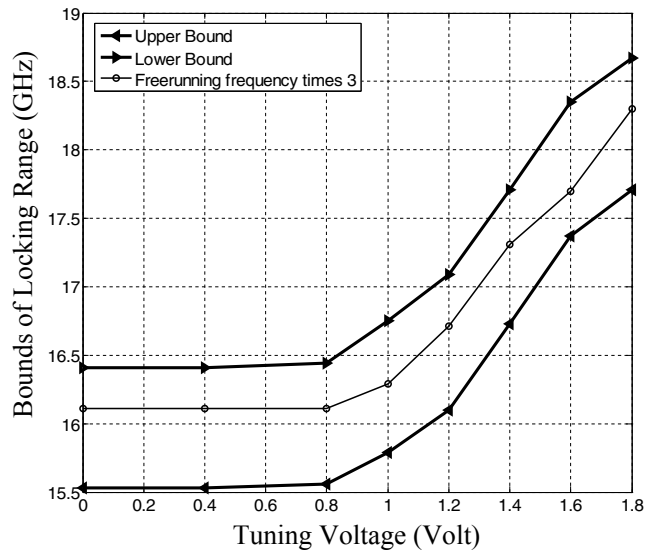


Figure 32.9.5: Measured tuning and locking range at 3.4dBm injected power.

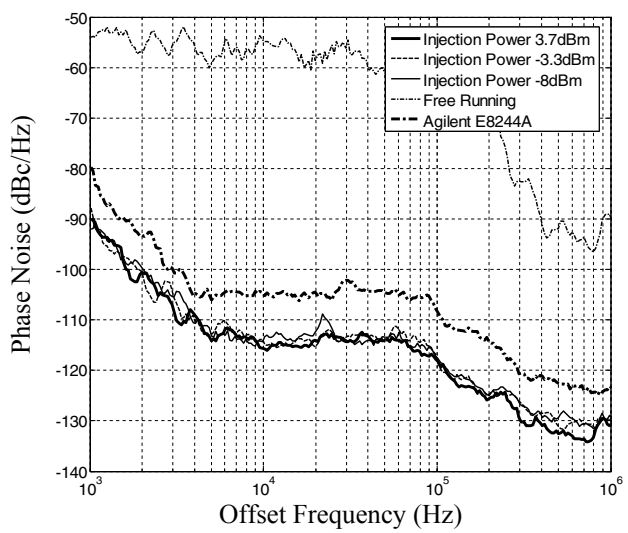


Figure 32.9.6: Measured phase noise at different injected power levels and free running.

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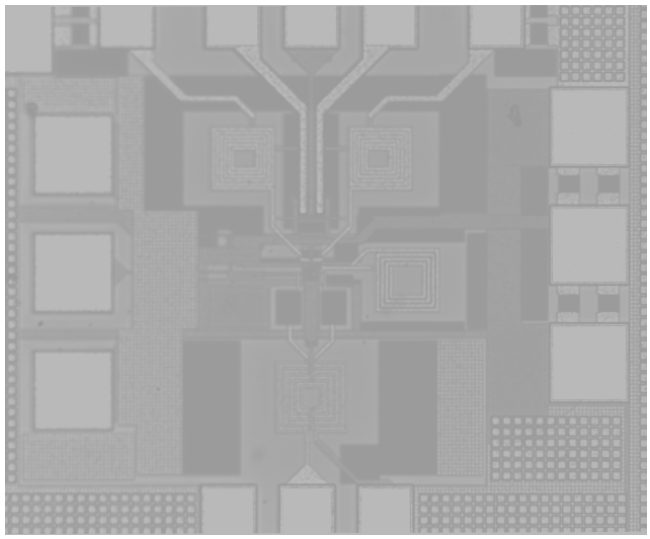

**Figure 32.9.7: Chip Micrograph.**

 